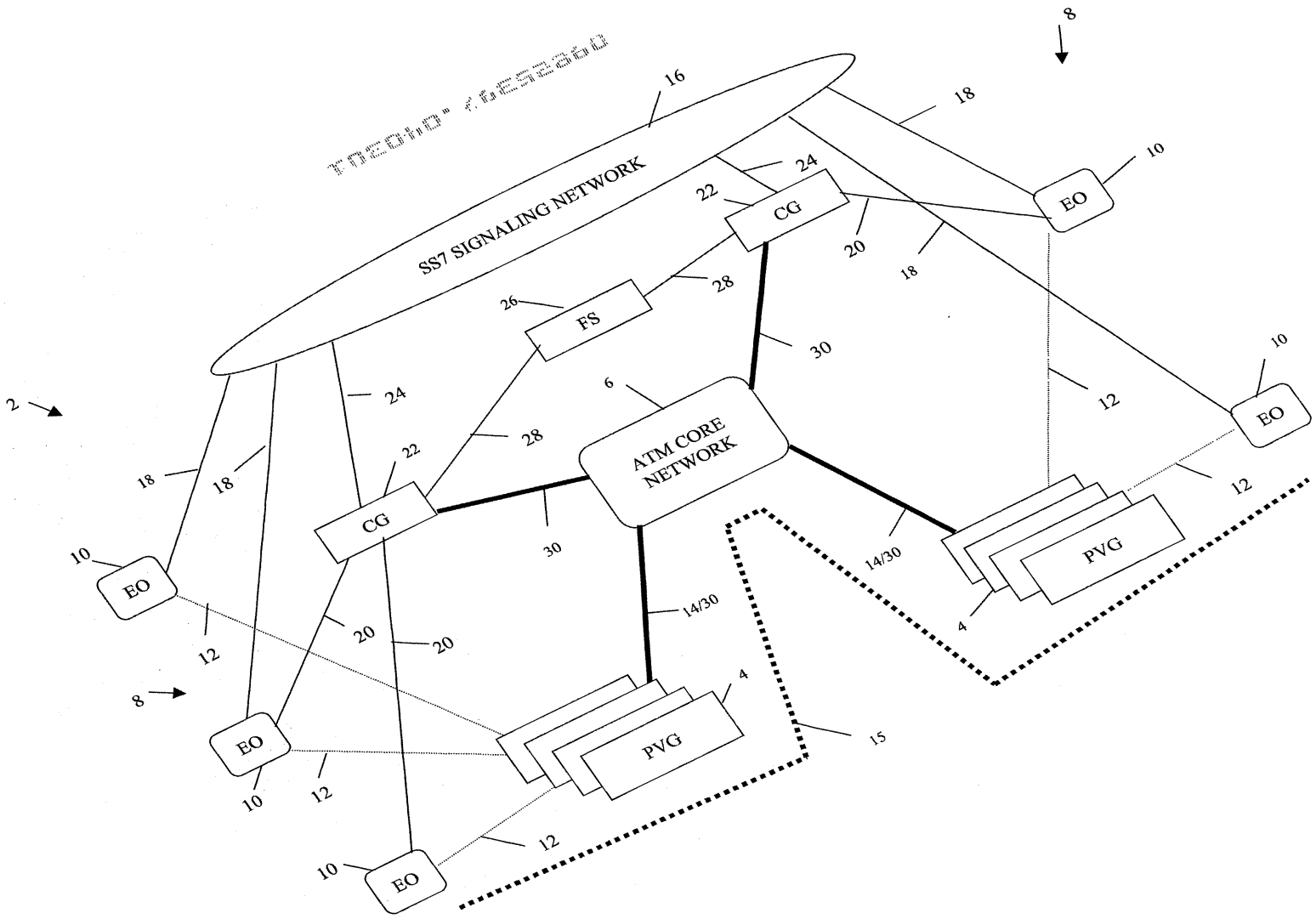
SS7 SIGNALING NETWORK
16
ATM CORE NETWORK
6
CG
22
FS
26
28
30
24
18
20
EO
10
12
PVG
4
14/30
15
2
8

FIG. 1

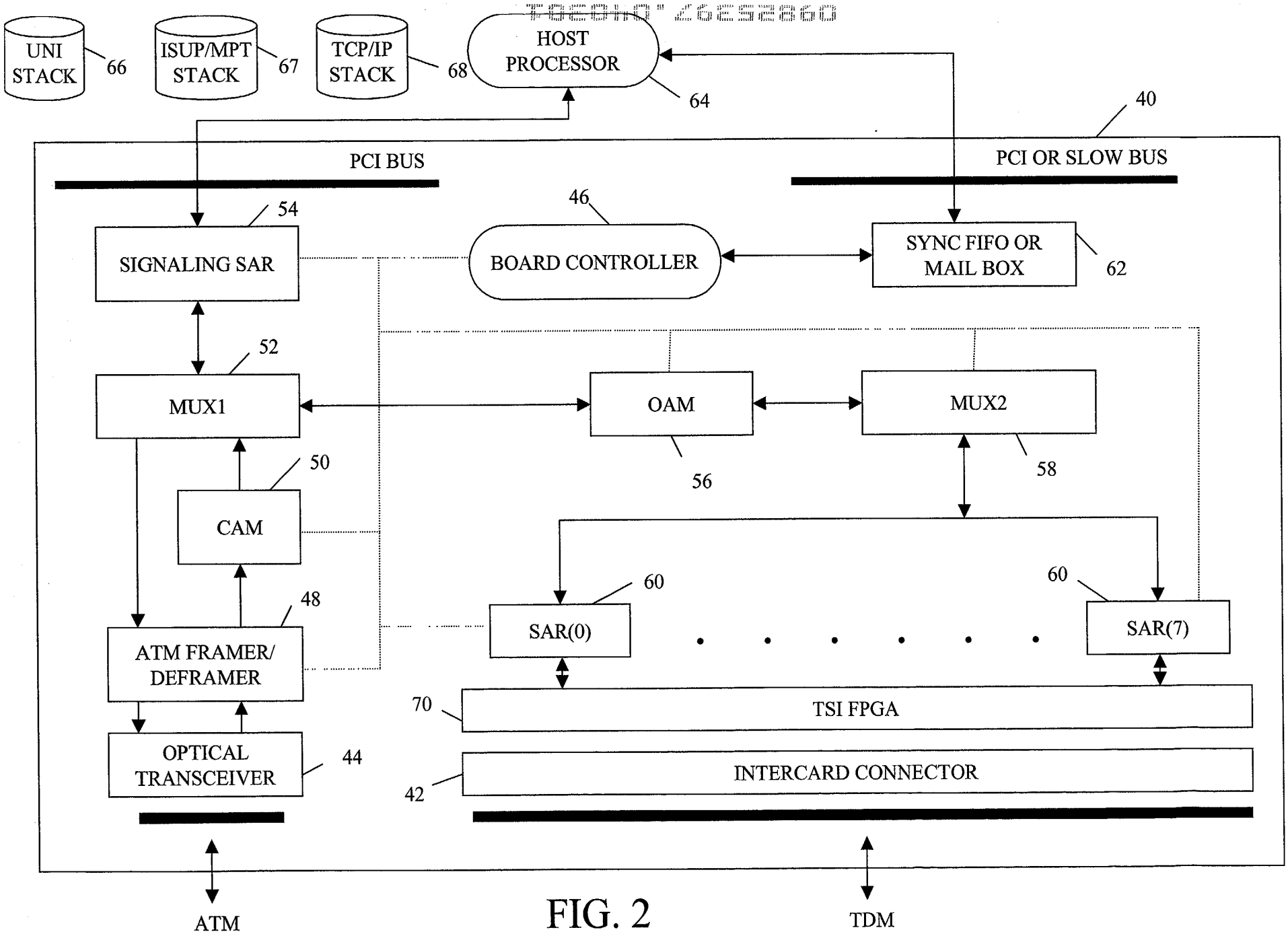
UNI STACK
66
ISUP/MPT STACK
67
TCP/IP STACK
68
HOST PROCESSOR
64
40
PCI BUS
PCI OR SLOW BUS
46
54
SIGNALING SAR
BOARD CONTROLLER
SYNC FIFO OR MAIL BOX
62
52
MUX1
OAM
MUX2
56
58
50
CAM
60
60
48
SAR(0)
SAR(7)
ATM FRAMER/ DEFRAMER
70
TSI FPGA
OPTICAL TRANSCEIVER
44
INTERCARD CONNECTOR
42
ATM
TDM

FIG. 2

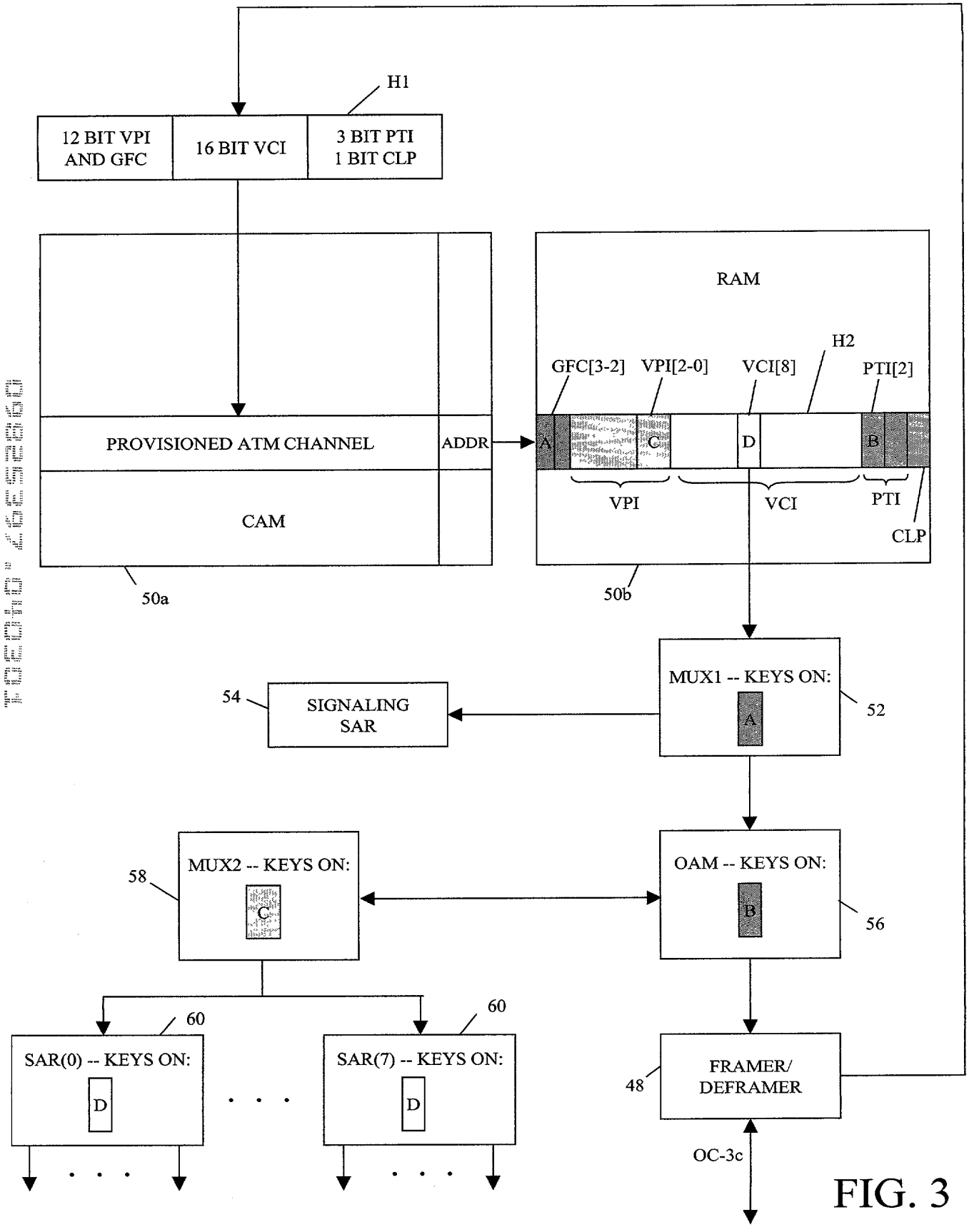
H1
12 BIT VPI AND GFC
16 BIT VCI
3 BIT PTI 1 BIT CLP
PROVISIONED ATM CHANNEL
ADDR
CAM
50a
RAM
GFC[3-2]
VPI[2-0]
VCI[8]
H2
PTI[2]
A
C
D
B
VPI
VCI
PTI
CLP
50b
MUX1 -- KEYS ON:
A
52
54
SIGNALING SAR
MUX2 -- KEYS ON:
C
58
OAM -- KEYS ON:
B
56
60
60
SAR(0) -- KEYS ON:
D
SAR(7) -- KEYS ON:
D
48
FRAMER/ DEFRAMER
OC-3c

FIG. 3

TOSHIBA 20E52860

CAM/RAM CELL HEADER TRANSLATION

HEADER FIELD	GFC 4-BIT		VPI 8-BIT		VCI 16-BIT			PTI 3-BIT		CLP	MUX1	OAM	MUX2	SAR
BIT FIELD POSITION	**3-2 (A)**	1-0	7-3	**2-0 (C)**	15-9	**8 (D)**	7-0	**2 (B)**	1-0	0	KEY ON **GFC[3-2]**	KEY ON **PTI[2]**	KEY ON **VPI[2-0]**	KEY ON **VCI[8]**
AAL1 USER CELLS	**0**	X	X	**ANY**	X	**1**	ANY	**0**	X	X	1-TO-4 DEMUX TO OAM	USER CELLS 0 PASS-THROUGH	1-TO-8 DEMUX	256 DS0 CHANNELS
SEG/END F5 OAM CELLS	**0**	X	X	**=USER**	X	**1**	SAME AS = USER	**1**	X	X	SAME AS ABOVE	OAM F5 CELLS ARE TERMINATED	N/A	N/A
SEG/END F4 OAM CELLS	**0**	X	ANY	**ANY**	X	**0**	SEG=3, END-TO-END=4	**1**	X	X	SAME AS ABOVE	OAM VCI=3 OR 4 ARE TERMINATED	N/A	N/A
SIGNALING HAIRPIN	**0**	X	ANY	**ANY**	X	**0**	ANY	**0**	X	X	SAME AS ABOVE	PASS THROUGH	1-TO-8 DEMUX	OAM QUEUE
UNHANDLED F5 OAM CELLS	**0**	X	X	**=USER**	0	**1**	SAME AS= USER	**0**	X	X	SAME AS ABOVE	PASS THROUGH	1-TO-8 DEMUX	OAM QUEUE
UNHANDLED F4 OAM CELLS	**0**	X	ANY	**ANY**	X	**0**	SEG=3, END-TO-END=4	**0**	X	X	SAME AS ABOVE	PASS THROUGH	1-TO-8 DEMUX	OAM QUEUE
AAL5 DATA CELLS	**1**	ANY	ANY	**ANY**	ANY	**A**	ANY	**0**	X	X	1-TO-4 DEMUX TO SIGNALING SAR	N/A	N/A	N/A
AAL5 F5 OAM CELLS	**1**	SAME AS AAL5 DATA CELLS						**1**	X	X	SAME AS ABOVE	N/A	N/A	N/A
AAL5 F4 OAMCELLS	**1**	ANY	ANY	**ANY**	ANY	**0**	SEG=3, END-TO-END=4	**X**	X	X	SAME AS ABOVE	N/A	N/A	N/A

FIG. 4

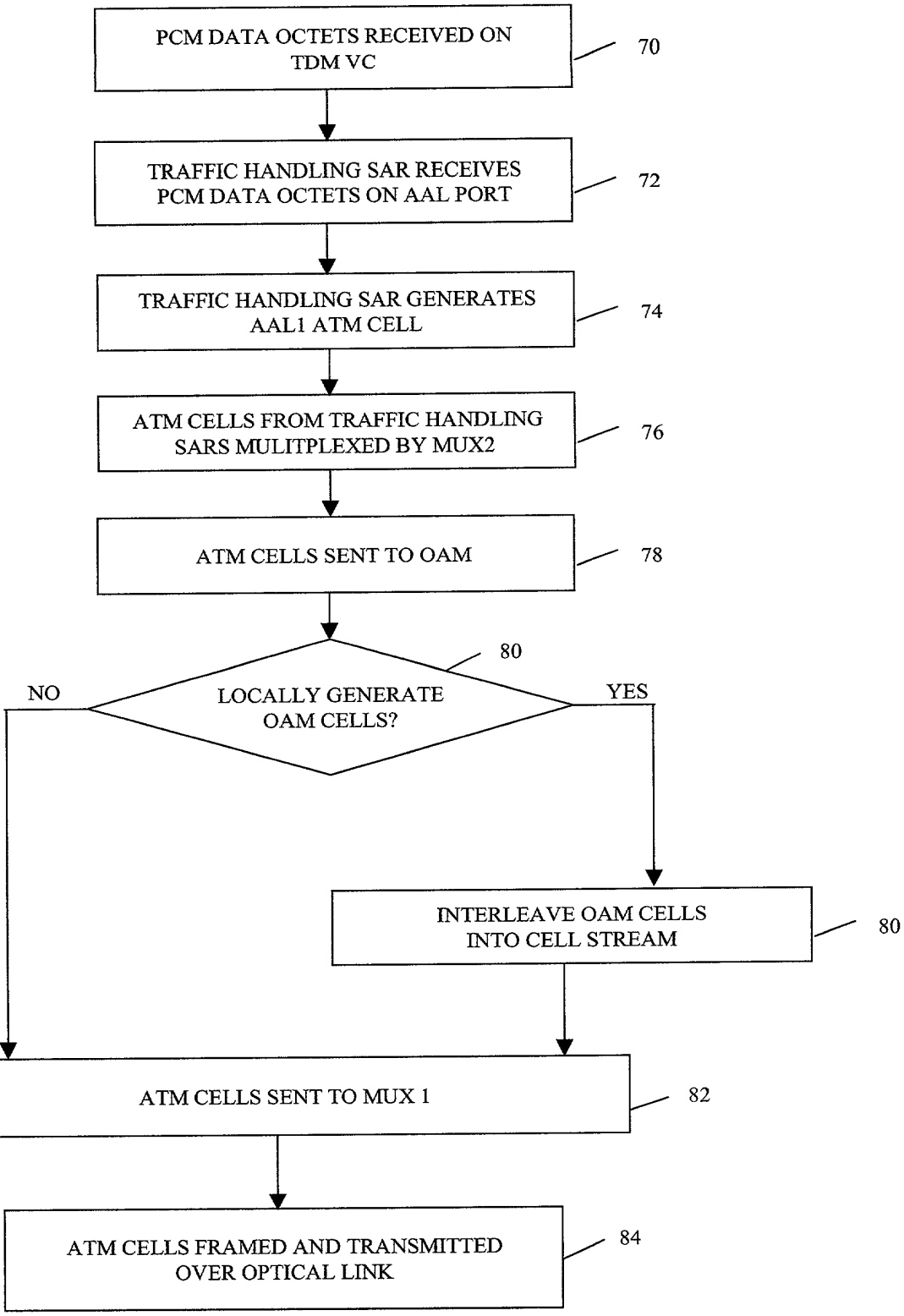
PCM DATA OCTETS RECEIVED ON TDM VC
70
TRAFFIC HANDLING SAR RECEIVES PCM DATA OCTETS ON AAL PORT
72
TRAFFIC HANDLING SAR GENERATES AAL1 ATM CELL
74
ATM CELLS FROM TRAFFIC HANDLING SARS MULITPLEXED BY MUX2
76
ATM CELLS SENT TO OAM
78
80
LOCALLY GENERATE OAM CELLS?
NO
YES
INTERLEAVE OAM CELLS INTO CELL STREAM
80
ATM CELLS SENT TO MUX 1
82
ATM CELLS FRAMED AND TRANSMITTED OVER OPTICAL LINK
84

FIG. 5

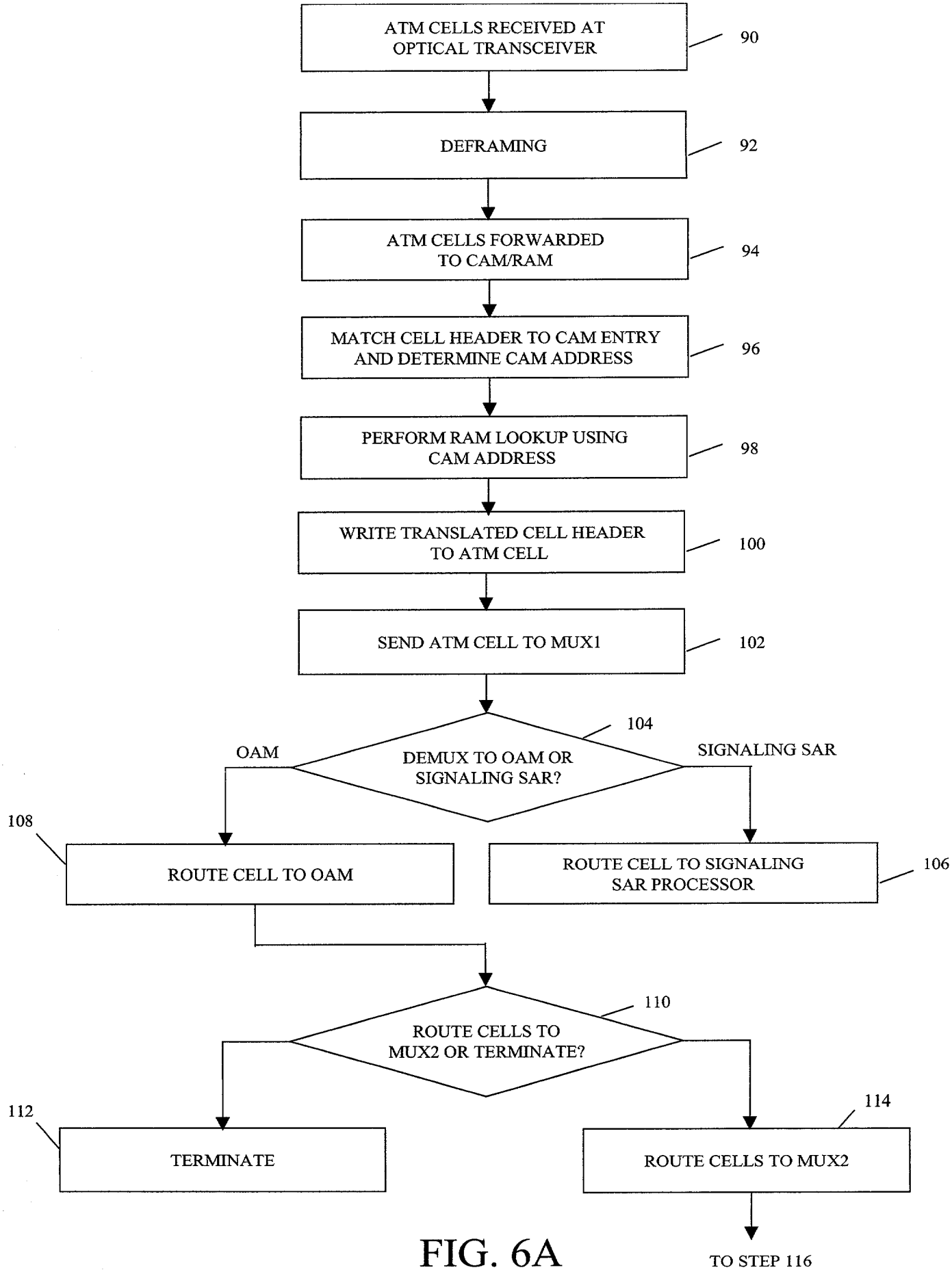
ATM CELLS RECEIVED AT OPTICAL TRANSCEIVER
90
DEFRAMING
92
ATM CELLS FORWARDED TO CAM/RAM
94
MATCH CELL HEADER TO CAM ENTRY AND DETERMINE CAM ADDRESS
96
PERFORM RAM LOOKUP USING CAM ADDRESS
98
WRITE TRANSLATED CELL HEADER TO ATM CELL
100
SEND ATM CELL TO MUX1
102
104
DEMUX TO OAM OR SIGNALING SAR?
OAM
SIGNALING SAR
108
ROUTE CELL TO OAM
ROUTE CELL TO SIGNALING SAR PROCESSOR
106
110
ROUTE CELLS TO MUX2 OR TERMINATE?
112
TERMINATE
114
ROUTE CELLS TO MUX2
TO STEP 116

FIG. 6A

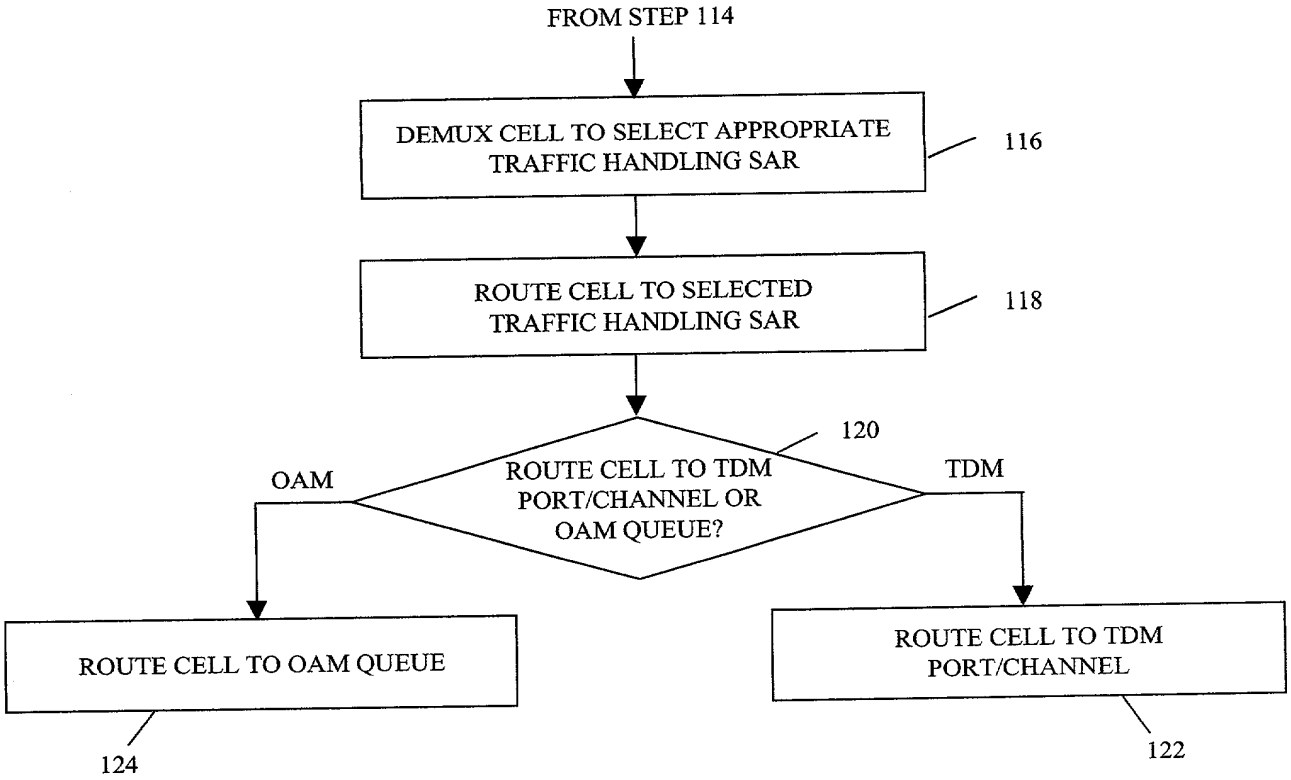
FROM STEP 114
DEMUX CELL TO SELECT APPROPRIATE TRAFFIC HANDLING SAR
116
ROUTE CELL TO SELECTED TRAFFIC HANDLING SAR
118
120
ROUTE CELL TO TDM PORT/CHANNEL OR OAM QUEUE?
OAM
TDM
ROUTE CELL TO OAM QUEUE
124
ROUTE CELL TO TDM PORT/CHANNEL
122

FIG. 6B